

CORNELL AERONAUTICAL LABORATORY, INC.
BUFFALO, NEW YORK 14221

FINAL PROJECT REPORT

STUDY OF THE APPLICATION OF PLANAR ELECTROLUMINESCENT
PANEL TECHNIQUES
(Project DISPLAY I)

CAL NO. IM-2280-E-1
FOR THE PERIOD: 13 JUNE 1966 - 13 JANUARY 1967
CONTRACT NO. NAS 5-10192
JANUARY 13, 1967

PREPARED BY: T. L. Robinson
T.L. Robinson
Project Engineer

APPROVED BY: C. W. Miller
C.W. Miller, Head
Electronics Research Department

Prepared for:
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

TABLE OF CONTENTS

<u>Section</u>	<u>Page</u>
I INTRODUCTION	I-1
A. Conventional Sandwich-Type EL Panels (SEL)	I-2
B. Planar Electroluminescent Panels (PEL)	I-3
II THEORETICAL AND EXPERIMENTAL ASPECTS OF PEL DISPLAYS	II-1
A. Operating Principles of the Basic PEL Cell.....	II-1
B. Experimental PEL Cells	II-4
1. Effect of Voltage on PEL Brightness Output ..	II-6
2. Brightness Dependence on Frequency	II-9
III EXPERIMENTAL DEVELOPMENT OF RAE-A ANTENNA BLOCK DIAGRAM SYSTEM DISPLAY	III-1
A. Art Work	III-1
B. Fabrication of Planar EL Module Substrates	III-6
1. Deposition of EL Phosphor	III-7
2. Testing of Planar EL Modules	III-9
IV THIN FILM DESIGN TECHNIQUES FOR PEL MOSAIC DISPLAYS	IV-1
V CONCLUSIONS AND RECOMMENDATIONS	V-1
APPENDIX I-1 Test Cell Performance Measurements	AI-1
APPENDIX II-1 Etching and Silk Screening Techniques	AII-1
REFERENCES	R-1

LIST OF ILLUSTRATIONS

<u>Figure</u>	<u>Title</u>	<u>Page</u>
I-1	Planar EL Panel	I-4
II-1	Field Lines in PEL and SEL Structures	II-2
II-2	Utilizing Fringe Field	II-2
II-3	B vs. Voltage	II-7
II-4	B vs. Voltage	II-8
II-5	B vs. Frequency	II-10
III-1	RAE-A Antenna Block Diagram	III-2
III-2	Art Work	III-3
III-3	Photo Reduction	III-4
III-4	Negative Retouching	III-5
III-5	Etching	III-7
III-6	Pre-Assembly	III-8
III-7	Module Attachment	III-10
III-8	Assembly Cross Section of Display	III-11
III-9	Testing Display	III-12
III-10	Electrical Terminal Code	III-13
IV-1	Detail of Insulated Cross-Over in X-Y Mosaic.....	IV-2

I. INTRODUCTION

This report summarizes the results of Project DISPLAY, a NASA-supported electroluminescent (EL) display program established for the purpose of meeting requirements for a visual display capable of presenting the status of electrical and mechanical systems in space vehicles. More specifically, the objective of this program was to conduct research and development in the application of planar electroluminescent panel techniques to system configuration displays. Also included were functional studies of CAL's basic planar electroluminescent cell as well as the development of techniques for the fabrication of multi-purpose displays containing storage capability, and building a breadboard model of one particular configuration display — the Antenna Block Diagram System for the RAE-A satellite. The purpose of this report is to give an account of the research by which the program objective was achieved.

Until several years ago, only one concept, i. e., that of the sandwich-type structure, was utilized in the design and fabrication of EL display panels employing intrinsic EL. The phenomena of intrinsic EL¹ (light emission from phosphor particles dispersed in a dielectric medium within an alternating electric field, also known as the Destriau Effect) was first reported by George Destriau in 1936. Recently, Cornell Aeronautical Laboratory, in an internally-sponsored research project, developed a unique and versatile concept for the design of EL panels, also based on intrinsic EL. This new idea is known as planar electroluminescence (PEL)². The state-of-the-art (conventional sandwich-type) EL panels, and the newly developed PEL panels will be defined in the following paragraphs.

CONVENTIONAL SANDWICH-TYPE EL PANELS (SEL)

The sandwich-type EL (shortened to SEL for brevity) concept is defined as a panel structure in which the phosphor-binder sheet combination is contained between two closely spaced electrodes, one of which must be light transmissive; the displacement current in a SEL is perpendicular to the plane of the electrodes. Since the discovery of intrinsic EL by Destriau, numerous electro-optical devices, based solely on the SEL structure, were devised including many variations of lamps, displays and light amplifiers. However, EL panel techniques based on the SEL structure have several inherent electrical and mechanical disadvantages which severely limit, or preclude their usefulness for certain requirements such as for high frequency operation, and for large EL display areas.

Typical SEL panels have capacitance values in the range of 100 picofarads per cm^2 , operate in the range of 100 to 600 volts at frequencies (the upper limit depending on the capacitance) from 60 Hz to 2000 Hz. At high frequency operation the reactive impedance of the SEL cell becomes small compared to the resistance of the light transmissive display electrode, thus resulting in an appreciable lateral voltage drop across the transparent conductor together with the generation of heat from I^2R losses. Such a voltage drop along the light transmissive conductor causes uneven light distribution across the panel due to the dependence of phosphor brightness on voltage. Furthermore, conventional SEL panels are difficult to prepare in the large sizes, sometimes required for displays. The main problems reside in: 1) depositing a thin, uniform layer of phosphor over the electrode area which must be free of pin holes and surface irregularities in order to prevent electrical breakdown; 2) the high resistance of the light transmissive electrode, and 3) high capacitance per unit area of the panel.

PLANAR ELECTROLUMINESCENT PANELS (PEL)

The approach described in this report for configuration displays is based on a new type of electroluminescent panel employing the planar concept. Electrodes and phosphor elements of the PEL panel are disposed on the same surface, and the displacement current is lateral with respect to the surface. This arrangement, shown schematically in its simplest form in Figure I-1, reduces the panel structure to a single layer having many highly desirable characteristics including:

1. High brightness resulting from high excitation frequencies and large display dimensions which are made possible by low capacitance per unit area of surface.
2. Low loss, which results from the use of high conductivity electrodes, i.e., the electrodes are not of the highly resistive, light transmissive kind common to sandwich-type EL panels.
3. Long life of the display because the phosphor may be replaced.
4. Low cost because conventional, highly developed, printed-circuit techniques can be used.
5. The application of phosphors in multi-colors over large areas by well-known silk screen techniques.

The manners in which the basic panel concept, shown in Figure I-1, was used for PEL configuration displays are described in the following sections.

Section II of this report will discuss the theoretical and experimental aspects of the development of PEL system configuration displays. The characteristics of EL light generated as a function of the operating conditions will also be included. Experimental development of an 18" x 24" breadboard for the RAE-A Antenna Block Diagram System will

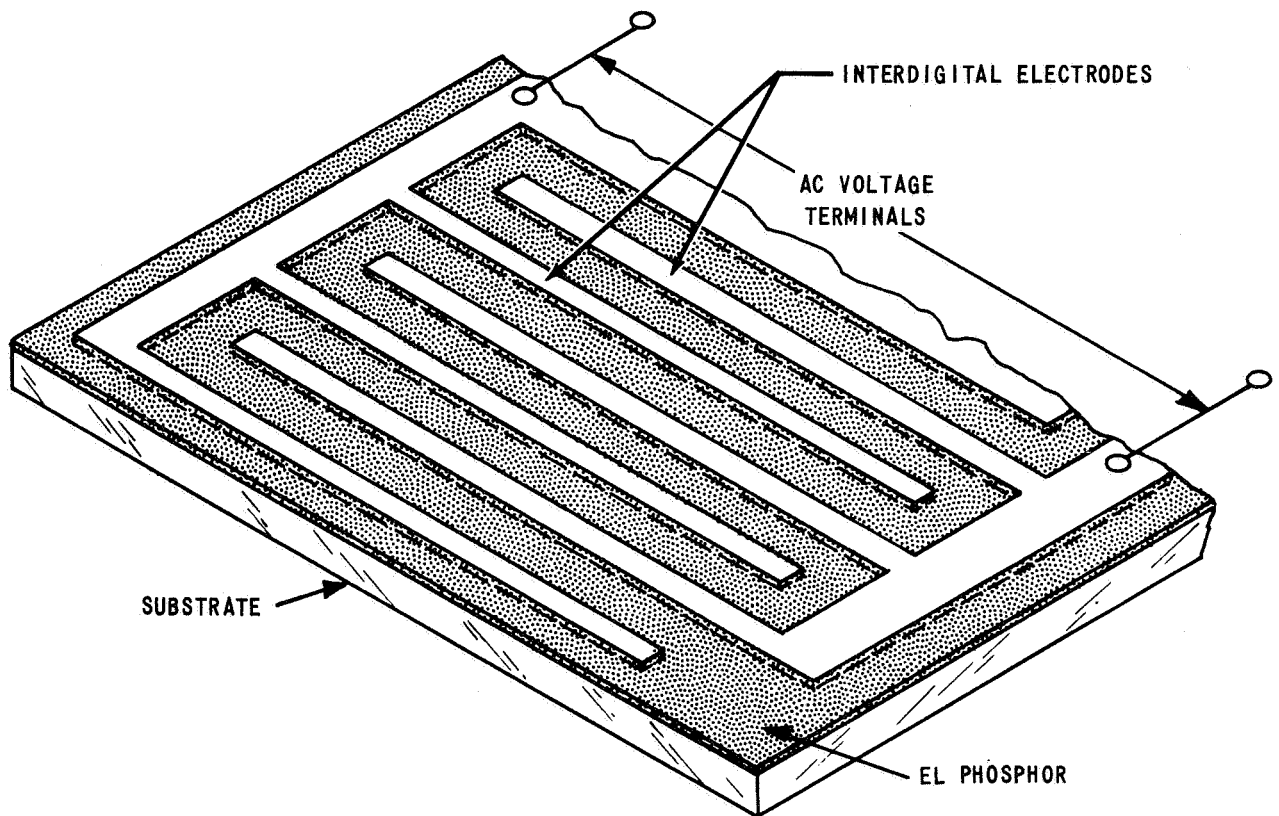


Figure I-1 PLANAR ELECTROLUMINESCENT PANEL

be detailed in Section III. Thin-film techniques are presented in Section IV for the fabrication of PEL mosaic type displays. Finally, in Section V, conclusions are drawn and recommendations made for future follow-on work concerned with EL displays.

II. THEORETICAL AND EXPERIMENTAL ASPECTS OF PEL DISPLAYS

A. OPERATING PRINCIPLES OF THE BASIC PEL CELL

The theoretical operation of PEL cells can be explained by comparing them with the operating fundamentals of conventional SEL cells, and noting the differences between the two. In Figure II-1 the electric field lines are shown for the PEL cell in A, and the SEL cell in B. It is seen that for the PEL cell, the electric field lines are parallel to the plane of the electrodes while for the SEL cell, the field lines are perpendicular to the plane of the electrodes. Also, the fringe field in the PEL structure is more pronounced than that in the SEL, but can be utilized to enhance the brightness if directed to traverse the phosphor particles by means of an overlay of high dielectric constant, light transmissive material as indicated in Figure II-2.

Phosphor-binder elements and ratios react in like manner in both types of EL cells. However, for the same phosphor-binder layer thickness, distinct reactions occur for each type of EL cell. On one hand for the SEL cell, the thickness of the phosphor-binder layer is significant in that it determines the electrode spacing, and hence the voltage required for a certain brightness output. On the other hand, the phosphor-binder layer thickness is not critical for the PEL cell since it does not determine the excitation voltage required; this requirement is set by the lateral spacing between the planar electrode terminals. Therefore the excitation voltage requirement in PEL cells is nearly independent of the phosphor layer thickness for thin layers. Theoretically, one should be able to choose the desired excitation voltage by simply adjusting the lateral spacing between the planar electrodes without regard to the phosphor layer thickness, except that the layer should not be "too" thick. In general, if the EL layer is too thick, light emission will be absorbed by the unexcited upper regions of the layer (those regions in the EL layer farthest away

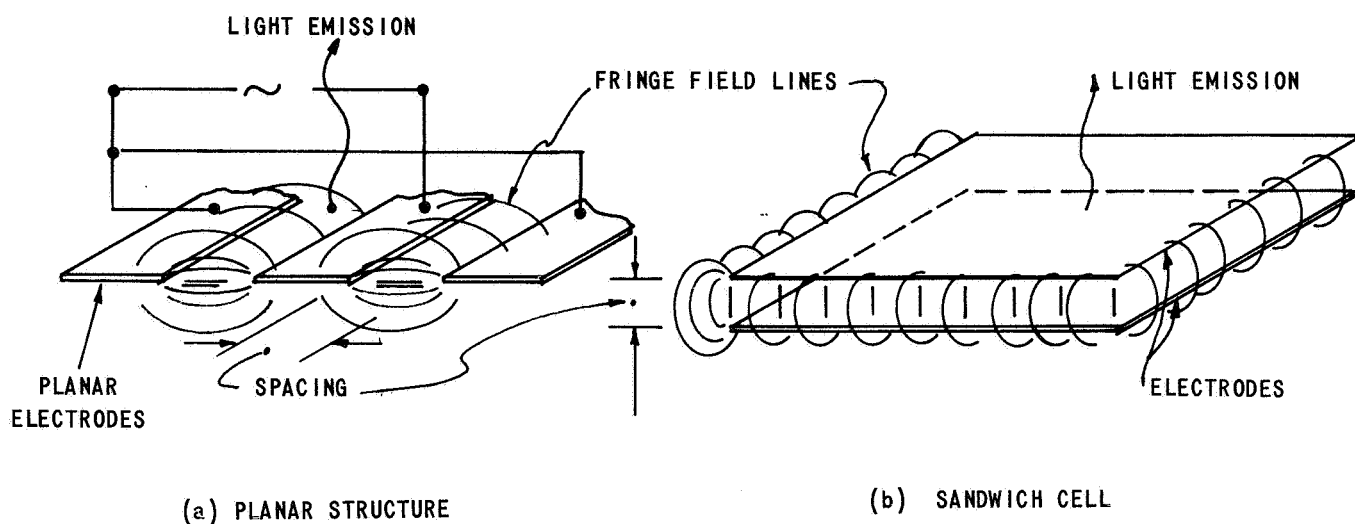


Figure II - 1 LINES IN PLANAR SANDWICH-TYPE STRUCTURE

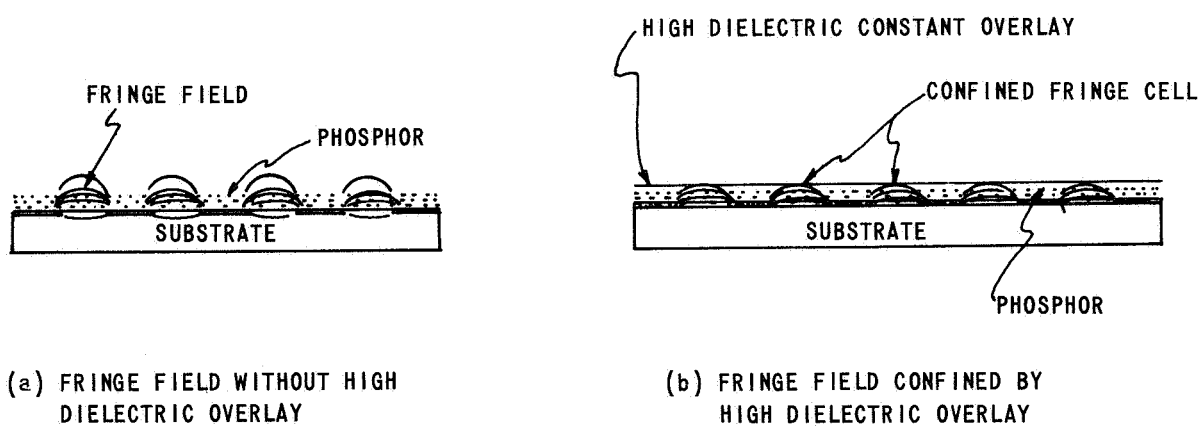


Figure II - 2 UTILIZING FRINGE FIELD WITH HIGH K OVERLAY

from the plane of the electrodes where the electric fringe field is weak), thus limiting the output. In transparent substrates, the light emission is seen from both sides of the PEL cell; the emission from the side contiguous to the phosphor-substrate interface would not suffer attenuation since the field strength here is greatest, and the EL light absorption due to thick phosphor layers is zero at this point.

B. EXPERIMENTAL PEL CELLS

Theoretical models on the mechanism of intrinsic electroluminescence in phosphors are well cited in the literature. (For example, see References 1, 3, and 4.) This section is concerned only with the application of the phenomenon of EL to planar cells under varying conditions of voltage, frequency, time and physical arrangement. In addition, the development and performance of experimental planar test cells will be reported.

A series of PEL test cells was fabricated and tested under varying conditions of voltage, frequency, time, and phosphor formulation. Of the PEL cells tested, certain ones (referred to as Cells Nos. 21, 22, 23 and 24 in the following discussion) more closely represent the characteristics of the PEL cells comprising the RAE-A Antenna Block Diagram Display than any other test cell made. Data from these selected cells are plotted and evaluated.

The instrumentation set-up for measuring the brightness output as a function of voltage, and frequency for various phosphors and binder ratios is shown in Appendix I-1.

Details on the fabrication procedures including etching, vacuum deposition, electroplating and the coating of the test cells are found in Appendix II-1.

Each of the PEL test cells (21, 22, 23 and 24) has phosphor-binder ratios of 3:1. The binder of the first three cells above employed a cyanoethyl starch, HD-27, obtained from the Hercules Powder Company. The fourth cell, No. 24, which served as an intensity demonstrator and which was delivered to NASA, utilized a binder consisting of a 1:1 ratio of HD-27 and of a cyanoethyl sugar (cyanoethyl sucrose) obtained from Eastman Chemical Division. Each test cell had electrode grid line widths and spacings of 4 mils (0.004") respectively. Test cells were constructed with green phosphor except Cell No. 22, which was a blue phosphor; the

phosphors were manufactured by the U.S. Radium Company. The two colors, green and blue represent the two-color combination used in the RAE-A Antenna Block Diagram Configuration Display; in the same manner the phosphor-binder ratios and the grid line widths and spacings are the same as in the breadboard display model.

The light emitting surfaces of test cells 21, 22 and 23 were divided into specially treated areas for the purpose of studying the effect on brightness output of the voltage gradient across the cell.

Test Cell 21 was divided into four areas: Area #1 consisted of only the basic green phosphor-binder layer (green phosphor plus HD-27 binder), while Area #2 had an overlay of clear mylar adhesive tape over the basic phosphor layer. Area #3 comprised the basic phosphor layer, but with the addition of clear mylar adhesive tape adhered to the cell surface with a film of cyanoethyl sucrose (CES), a viscous, optically clear, high-dielectric material with a dielectric constant between 25 and 40. In Area #4, the basic phosphor layer was overlaid with a thin film of CES only.

Test Cell #22, with a basic blue phosphor-binder layer, was composed of two areas. One area was covered with a clear strip of mylar adhesive tape adhered to the cell surface with a film of CES; the other half of the cell consisted of the uncovered basic phosphor layer.

Test Cell #23 was treated in the same way as Cell #22, but the basic phosphor layer was a green formulation.

Test Cell #24 did not have any treatment over its basic green phosphor layer.

1. Effect of Voltage on PEL Brightness Output

Considering Cell #21 with the 4 treated areas, Curve 1 in Figure II-3 represents both Areas 3 and 4 having overlays of CES, and CES-bonded clear mylar tape respectively. Curve 2 in the same figure is a representation of Area 1 which had no overlay, and Area 2, which had only the mylar pressure sensitive tape overlay. It can be observed by comparing Curve 1 with Curve 2 in Figure II-3 that the phosphor surface areas that were treated with the high dielectric constant CES film over the basic (cyanoethyl starch-phosphor formulation) EL layer has a sensitizing effect on the phosphor brightness output. For the voltage gradient between 50 volts per mil (0.001") and 75 volts per mil in the phosphor, B is seen to be approximately 35 percent greater for the CES treated areas. As the field strength is increased to 125 volts per mil, B for Curve 1 also increases by greater than 50 percent over B for Curve 2.

Data for test cells #22, 23 and 24 are plotted in Figure II-4. Cell #22, with a blue phosphor formulation exhibits the lowest B value of the test group reported here, indicated by Curves 22-1 and 22-2. The untreated basic EL area of the cell, when treated with the CES-tape overlay raised the output emission by approximately 350% at a field strength of 125 volts per mil. With lower voltage gradients, the percentage B increase is much greater, i.e., at a field level of 50 volts per mil, the brightness due to the treated area is intensified greater than ten fold for the blue phosphor.

The voltage effect on the green phosphor formulations, according to the data, was not as pronounced as that for the blue phosphor formulations as will be shown next with reference to the green test cells #23 and #24. Inspection of Curves 23-1 and 23-2 at the 125 volts/mil point, and the 50 volts per mil point show that the voltage dependence is nearly constant at about 150% greater enhancement of brightness for the CES treated phosphor area. Curve 24, a green phosphor cell with a 1:1 ratio of CES and HD-27 and no overlay, represents the highest B formulation.

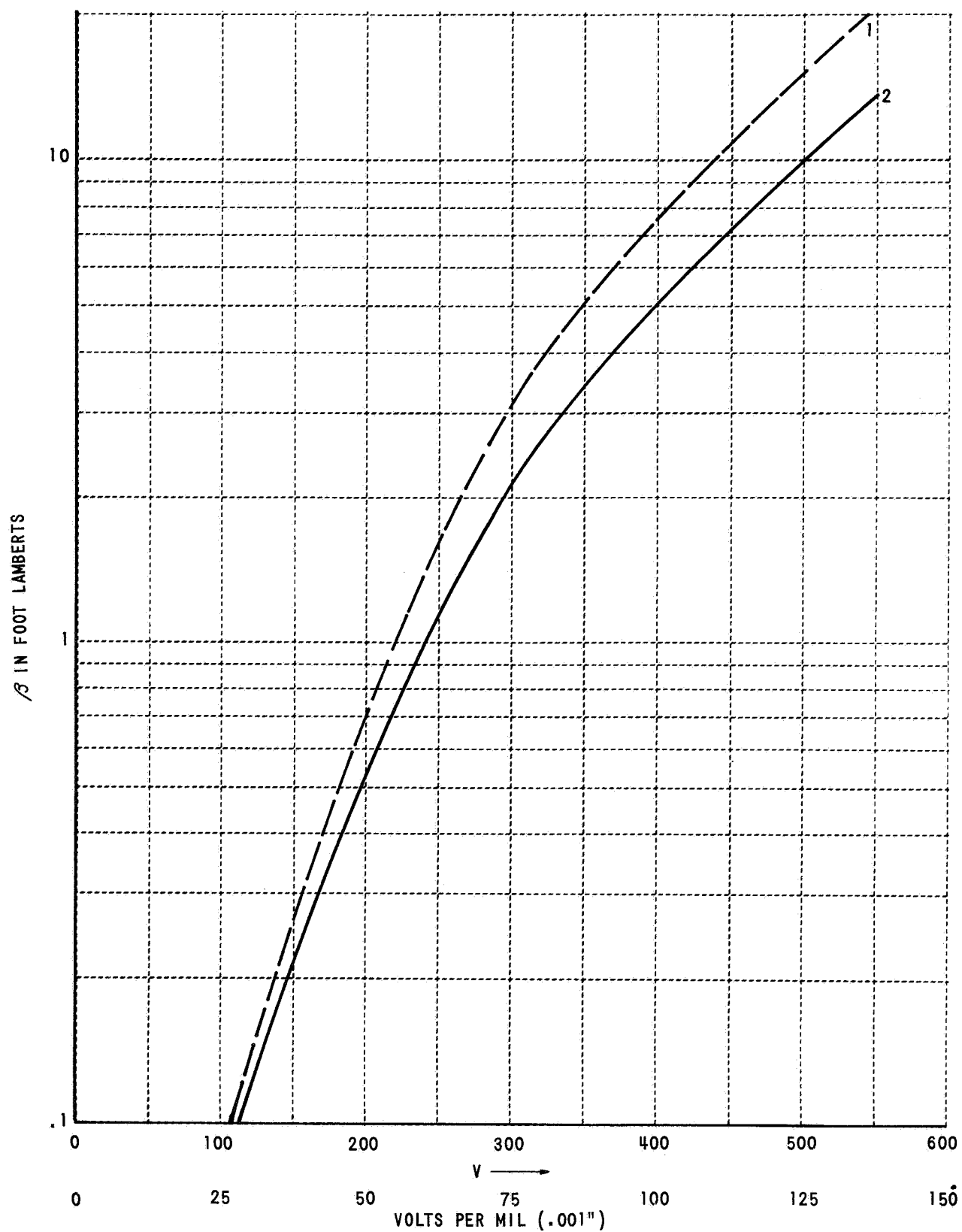


Figure II-3 B vs VOLTAGE

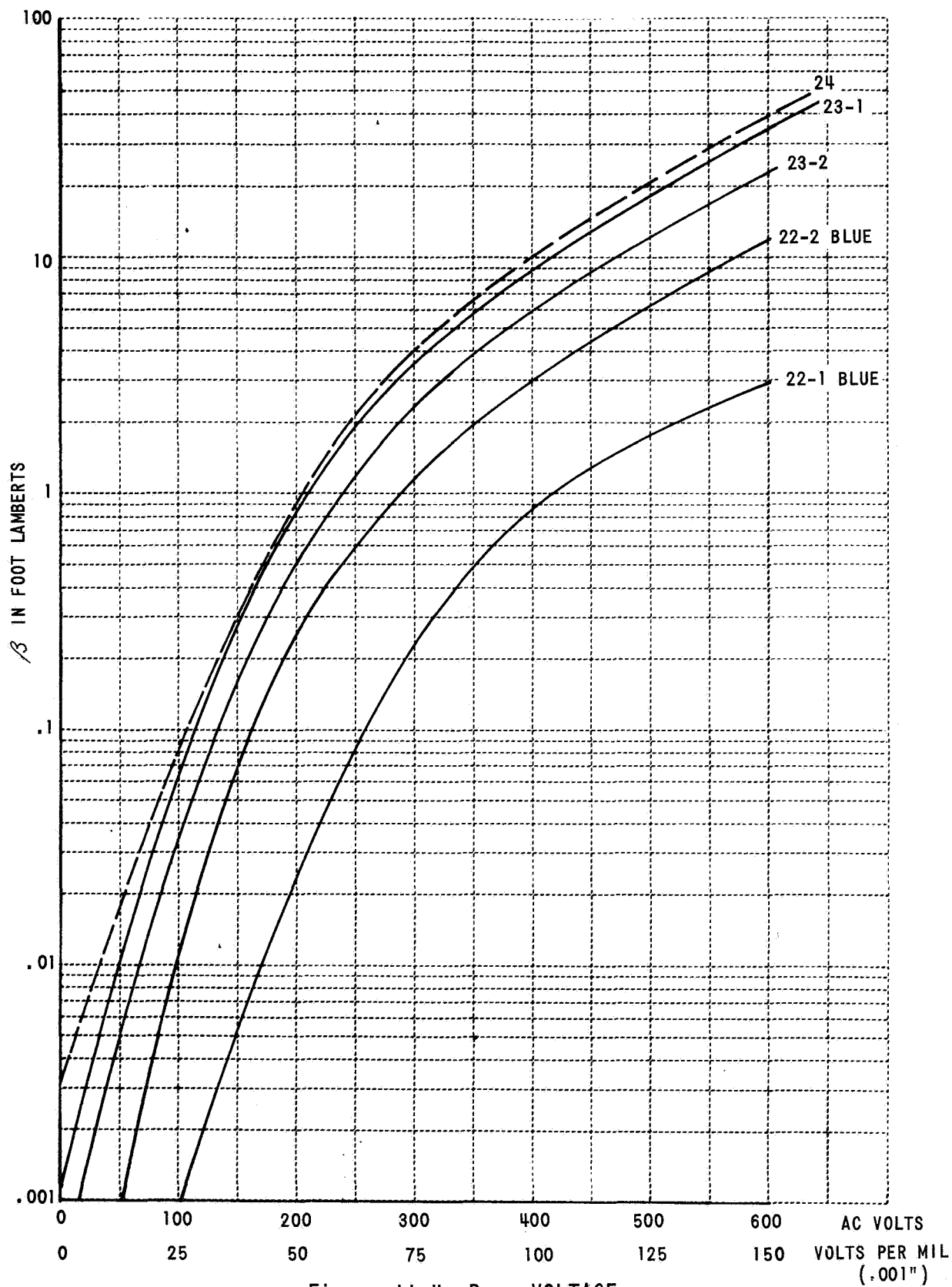


Figure II-4 B vs VOLTAGE

The formulation in test cell #24 (the intensity demonstrator shipped to NASA) represents the phosphor-binder incorporated in the RAE-A Antenna Block Diagram Configuration Display breadboard.

2. Brightness Dependence on Frequency

Figure II-5 shows a family of curves for test cells #21 (green) and for #22 (blue) which indicate the B dependence on frequency for treated and untreated EL surface areas. The curves show that the EL phosphor surface treatment has little effect on the shape of the B vs. f curve for frequencies greater than 300 Hz. In general, the curves present a linear dependence of B on frequency. Curves 1, 2 and 4 exhibit the same slope, while the slope of Curve 3 is slightly flatter, indicating a smaller degree of B dependence on frequency. The difference in the slope of Curve 3 is apparently due only to the absence of the high dielectric surface treatment with the CES overlay.

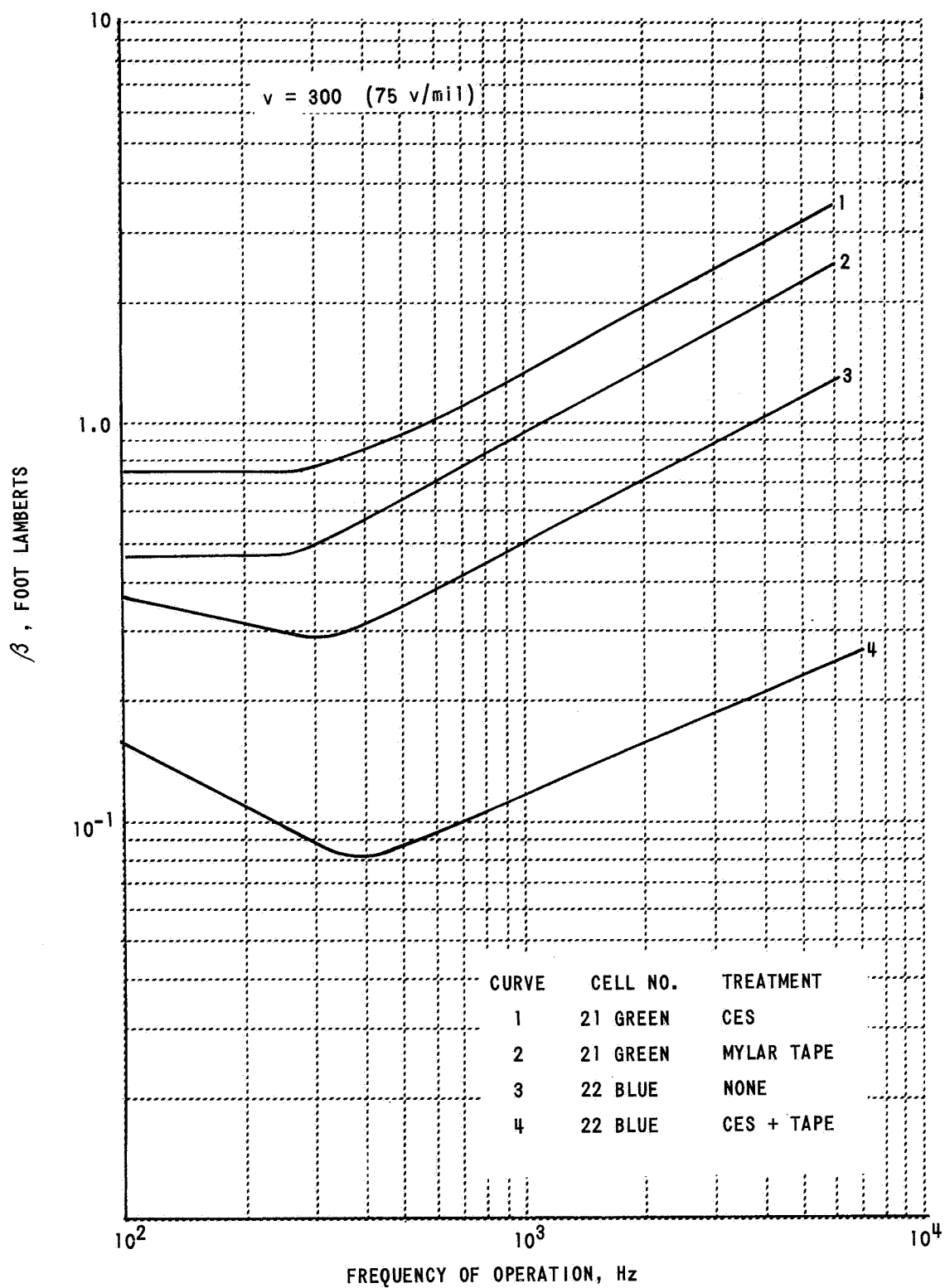


Figure II - 5 BRIGHTNESS vs FREQUENCY

III. EXPERIMENTAL DEVELOPMENT OF RAE-A ANTENNA BLOCK DIAGRAM SYSTEM DISPLAY

The development of a planar, two-color electroluminescent breadboard of the RAE-A Antenna Block Diagram Display (see Figure III-1) involved the following steps and procedures:

1. Development of the art work.
2. Fabricating the planar EL cell substrates.
3. Deposition of the EL phosphor in two colors.
4. Testing of each display module and final assembly.

A. ART WORK

The RAE-A Antenna Block Diagram was laid out on the drafting board and broken up into 18 separate functional module areas with several small interconnecting splices. Each separate module was drawn up to 50 times actual size, as shown in Figure III-2, and then reduced photographically to the actual size by means of photomechanical techniques. Figure III-3 shows an enlarged piece of art work in a vacuum frame, which is to be reduced photomechanically. The actual size negative masters were retouched to clean up the clear areas and opaque pin holes in order to preclude shorted grids or open conductors in the etched grid pattern (see Figure III-4).

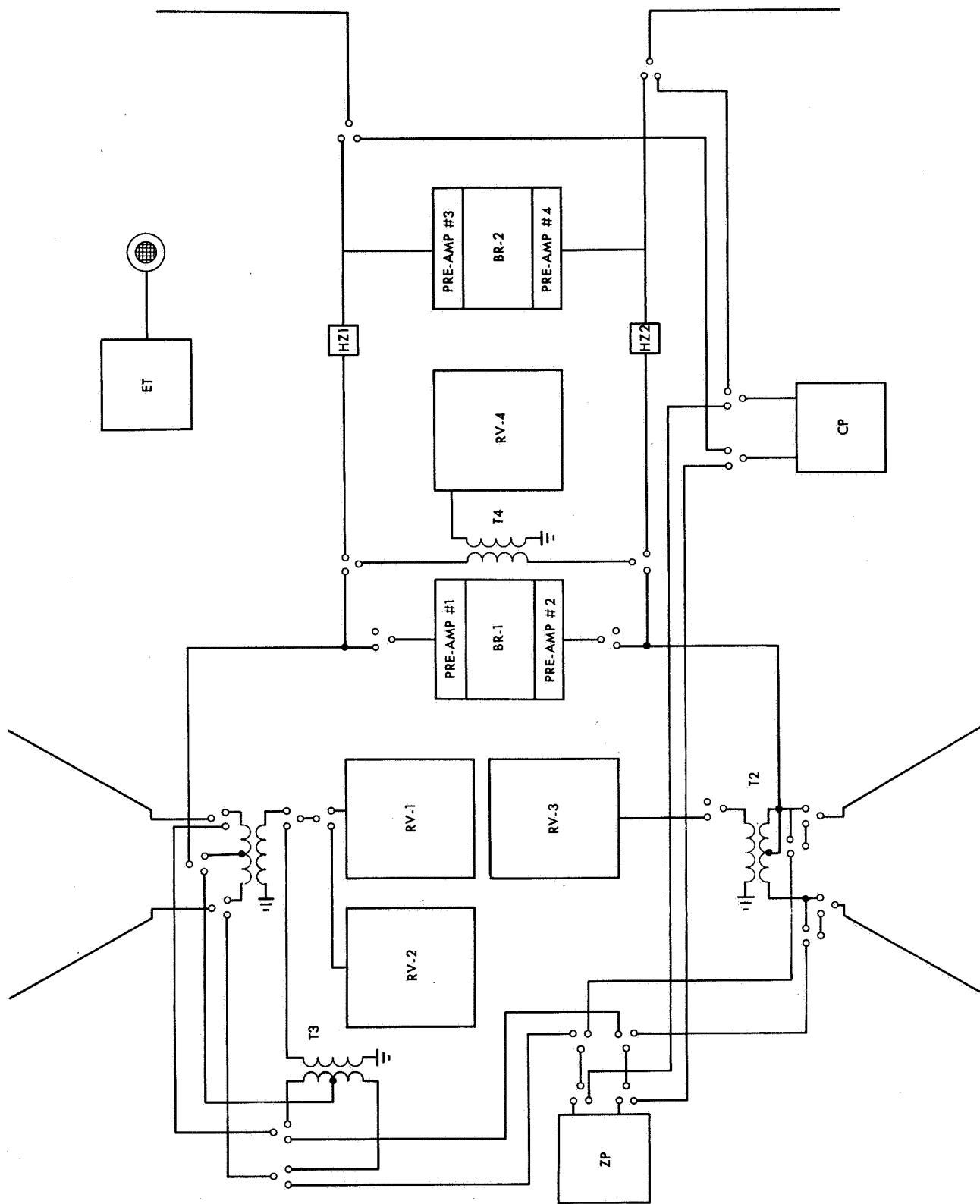


Figure III-1 RAE-A ANTENNA BLOCK DIAGRAM

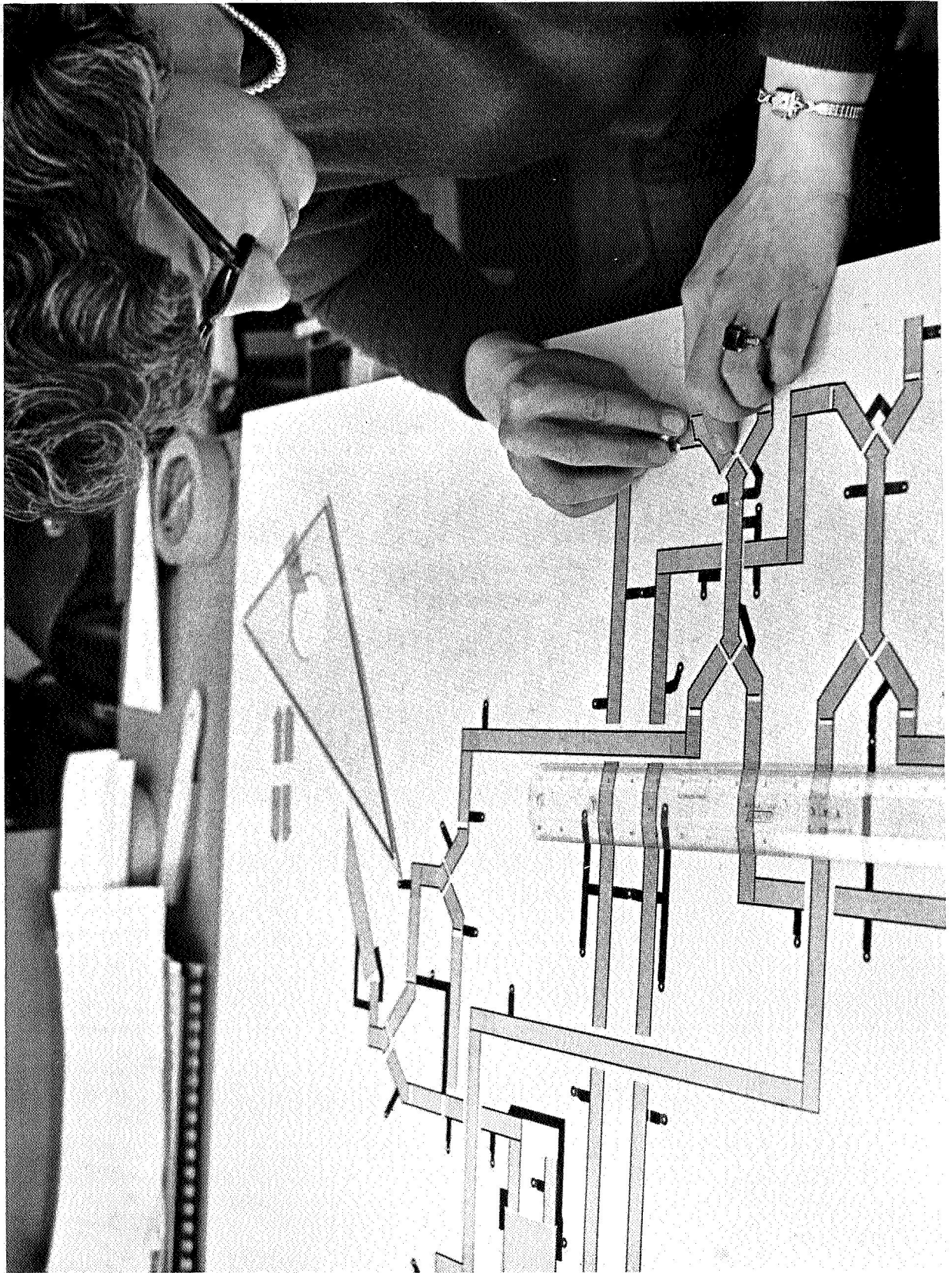


Figure III-2 ART WORK



Figure III-3 PHOTO REDUCTION

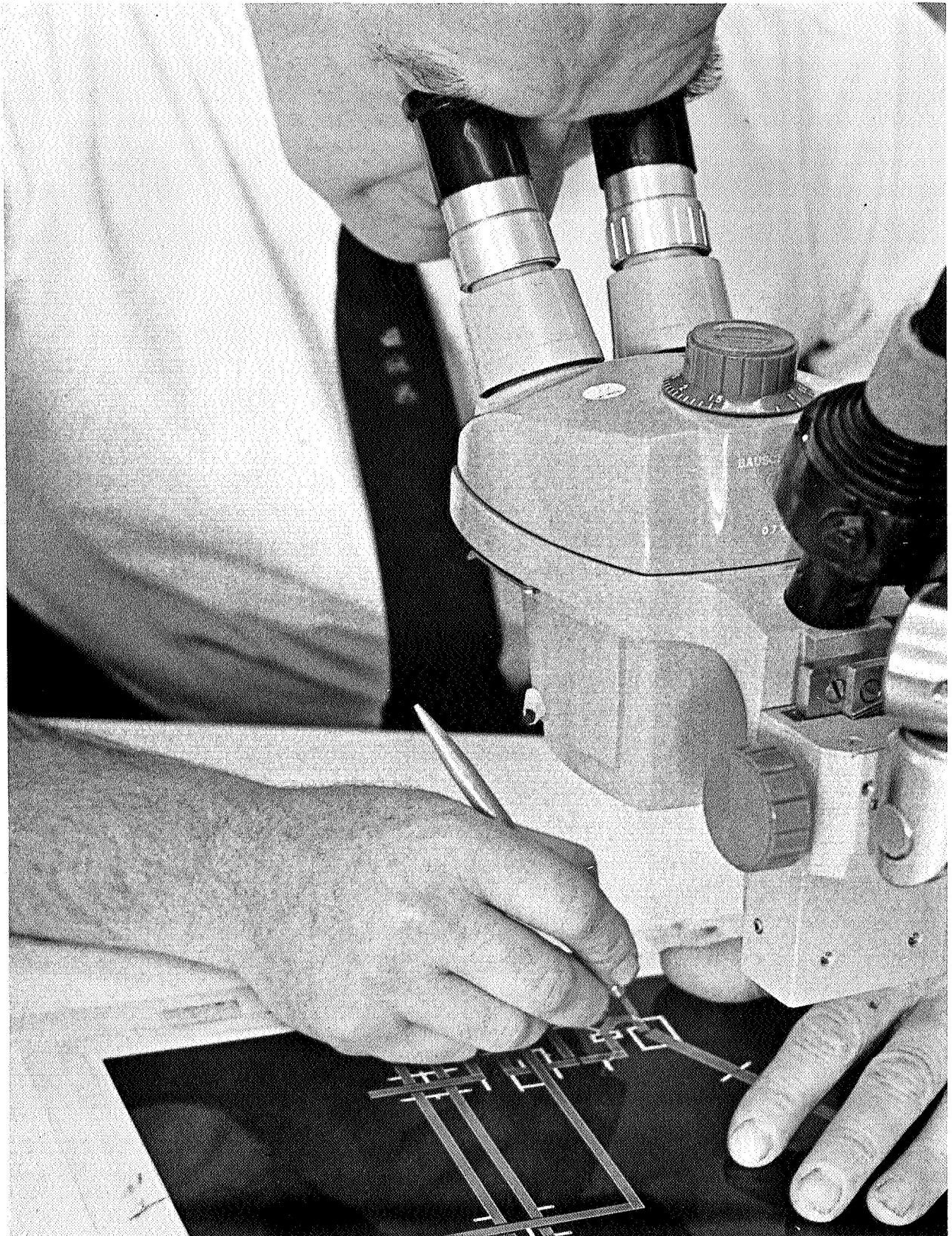


Figure III-4 NEGATIVE RETOUCHING

B. FABRICATION OF PLANAR EL MODULE SUBSTRATES

Following the preparation of actual size photographic transparencies, the next step in the fabrication of the planar EL modules was to photosensitize the surfaces of specially prepared 1/16" thick copper clad, epoxy fiberglass substrates; details on the preparation and etching of the substrates appear in Appendix II-1. After the etching operation (Figure III-5) the resist was removed and the modules were inspected for shorted or open conductors with the aid of a low power microscope. Shorted conductors were repaired by cutting out the shorts with a sharp frisket knife. Modules were rejected if open conductors were found. If the etched substrate passed inspection, eyelets were applied to the terminal lands, and then the surface was degreased followed by the application of an insulating layer of Kodak Photo Resist (KPR) by spraying. The photo-sensitive resist was dried under safe-light conditions and then exposed through a photographic transparency to polymerize the insulation in order to facilitate the soldering of lead wires which were used for connecting the module terminals to the printed circuit "mother" board. "Mother board" is a term used in the printed circuit art to designate a master circuit array printed on a substrate large enough to accommodate and interconnect all modules in a functional assembly.

Before the phosphor was deposited on the surface of the planar EL modules, they were laid out in jig-saw fashion on a table top to determine the final position of each module. (See Figure III-6.) A photographic pattern of the mother board wiring layout was used as a registration pattern for precisely locating the position of each planar EL module so that when holes were drilled into the mother board at terminal land locations, the modules could be simply "plugged" in. A photographic mask, shown in the lower right-hand corner of Figure III-6 was made to mask the nonelectroluminescent areas of the RAE-A Antenna Block Diagram Display, and to improve contrast and aesthetic quality.

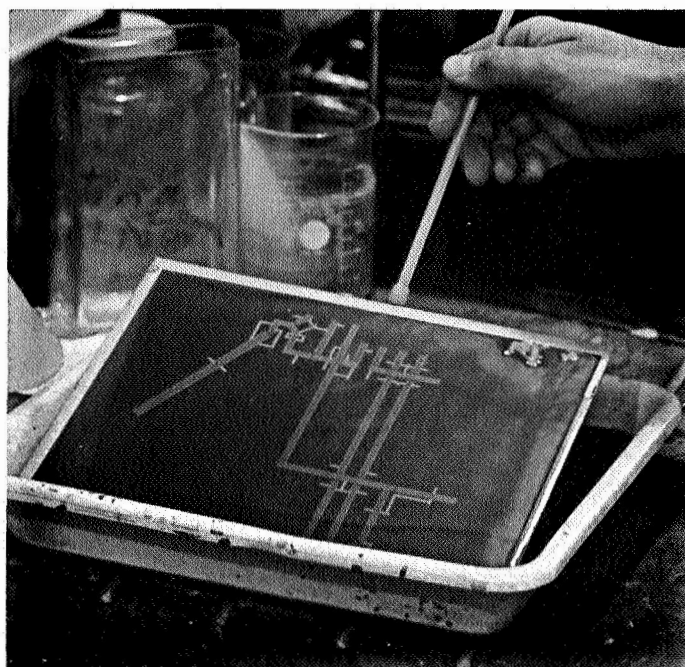


Figure III-5 ETCHING

1. Deposition of EL Phosphor

The phosphor-binder formulations utilized in the RAE-A Antenna Breadboard Display was composed of a 1:1 mixture of HD-27, and cyanoethyl sucrose (CES), thinned to working consistency with a 50-50 solution of dimethylforminide and acetone. To this 1:1 mixture of HD-27 and CES was added three parts by weight of electroluminescent phosphor. A small amount of an inert suspending agent (silicic acid in powdered form) had to be added to the green phosphor mixture for ease in silk screening. The blue phosphor was finer grained and did not need a suspending agent.

Silk screen application of the phosphor formulation on the printed substrates was accomplished by placing the work with the lead wires bent parallel to the surface on a vacuum table top to hold it down. One end of the registered silk screen frame was then loaded with a predetermined amount of the phosphor formulation in a paste-like consistency,

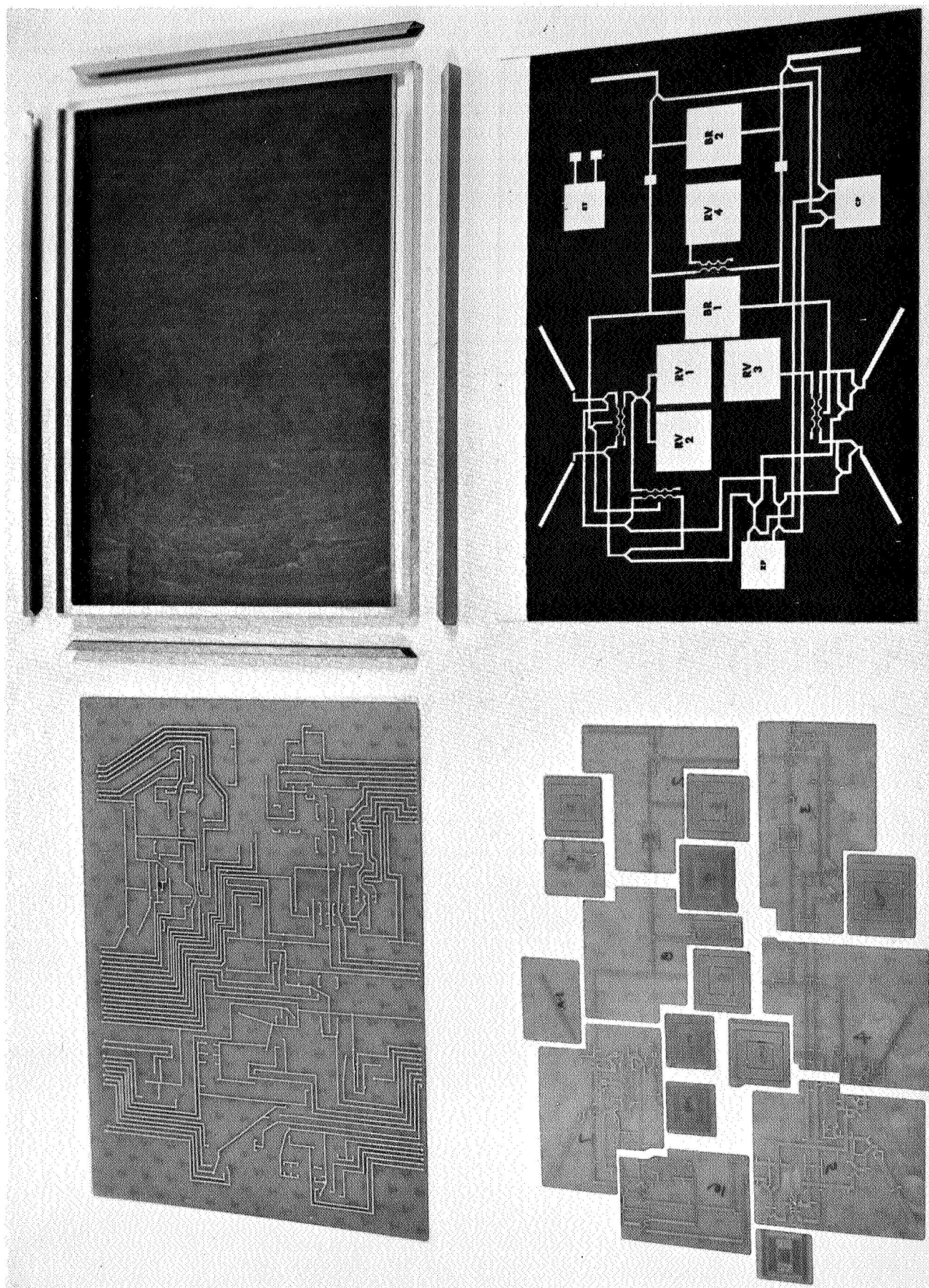


Figure III-6 PRE-ASSEMBLY

the screen was then lowered in position over the substrate and the squeegee moved across the screen to force the phosphor mixture through openings in the screen pattern on to the work surface below. Usually, one back and forth stroke is sufficient to deposit a smooth, even layer of phosphor providing the proper consistency is maintained.

In applying two colors to the modules, one color was silk screened at a time and the coating allowed to dry before application of the second color.

2. Testing of Planar EL Modules

Each module was tested for EL emission after drying in a dust-free atmosphere, and then plugged into the mother board and the leads connected by soldering (see Figure III-7). After all EL modules and interconnecting EL strips were soldered to the mother board, a final overall electrical test of each of the 53 functions was made for EL emission; then the breadboard was assembled in the frame (see Figure III-8) and once again given a final electrical test as shown in Figure III-9.

The electrical terminal number code for the RAE-E Antenna Block Diagram is shown in Figure III-10.

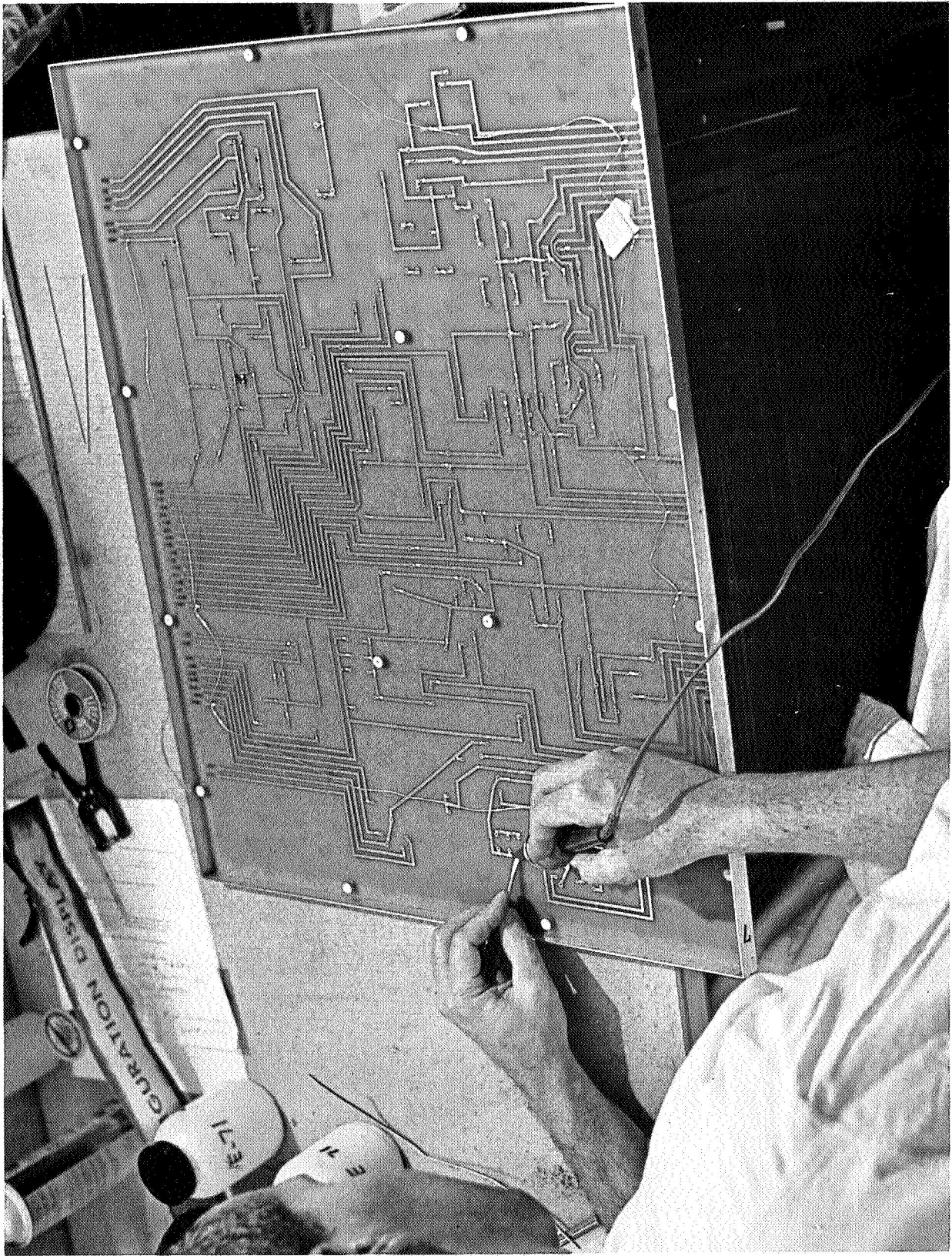


Figure III-7 MODULE ATTACHMENT

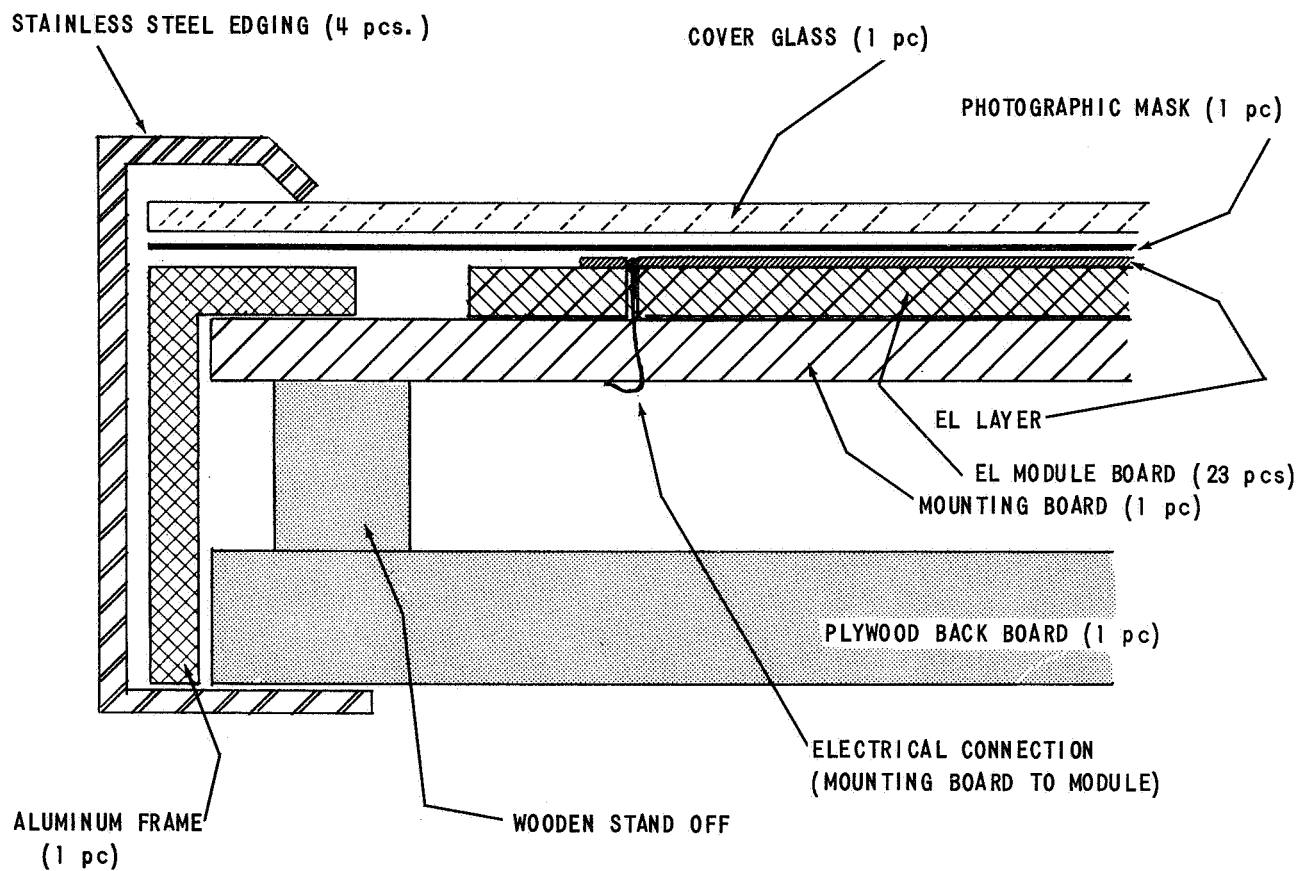


Figure III-8 ASSEMBLY CROSS SECTION OF DISPLAY

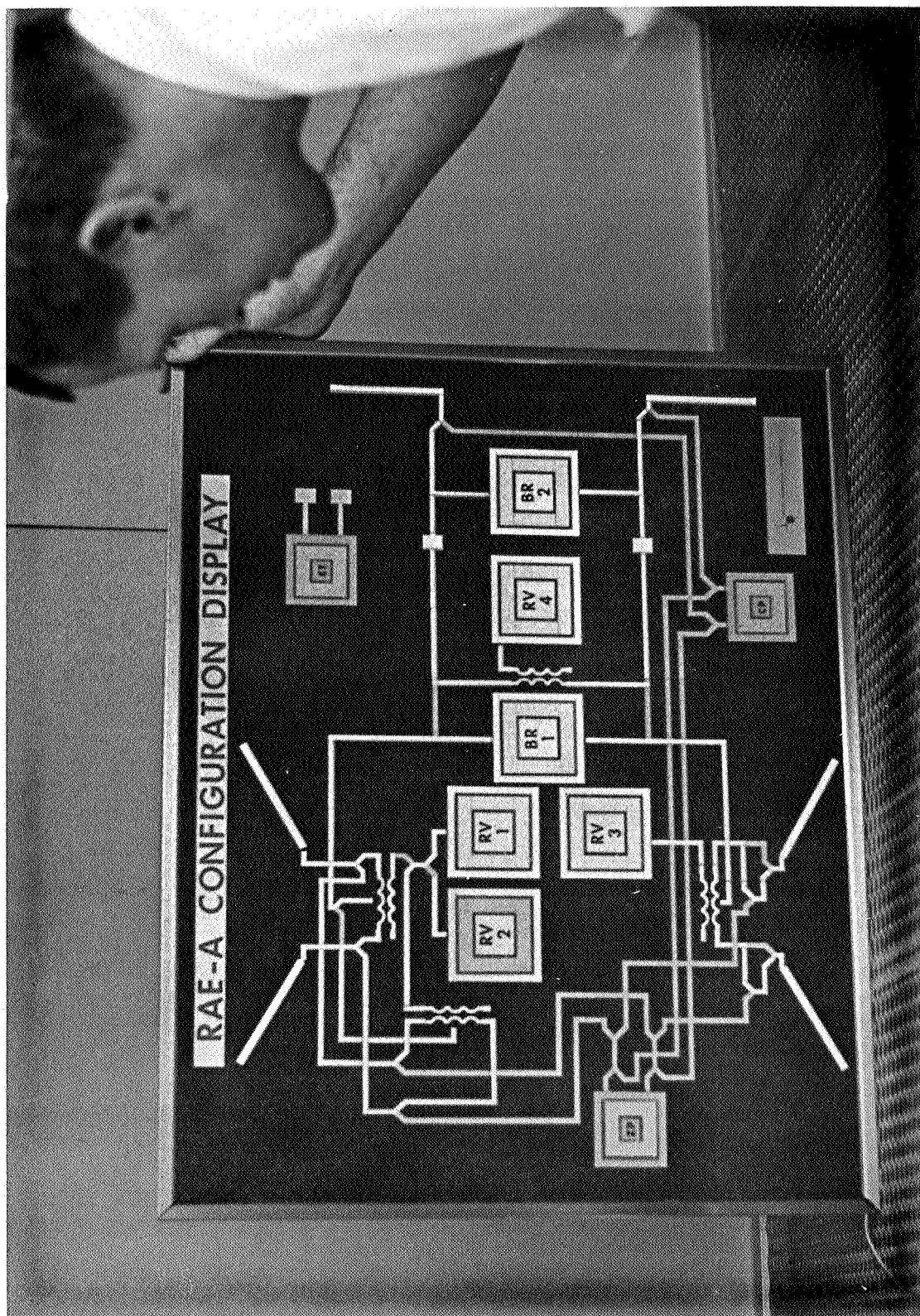


Figure III-9 TESTING DISPLAY

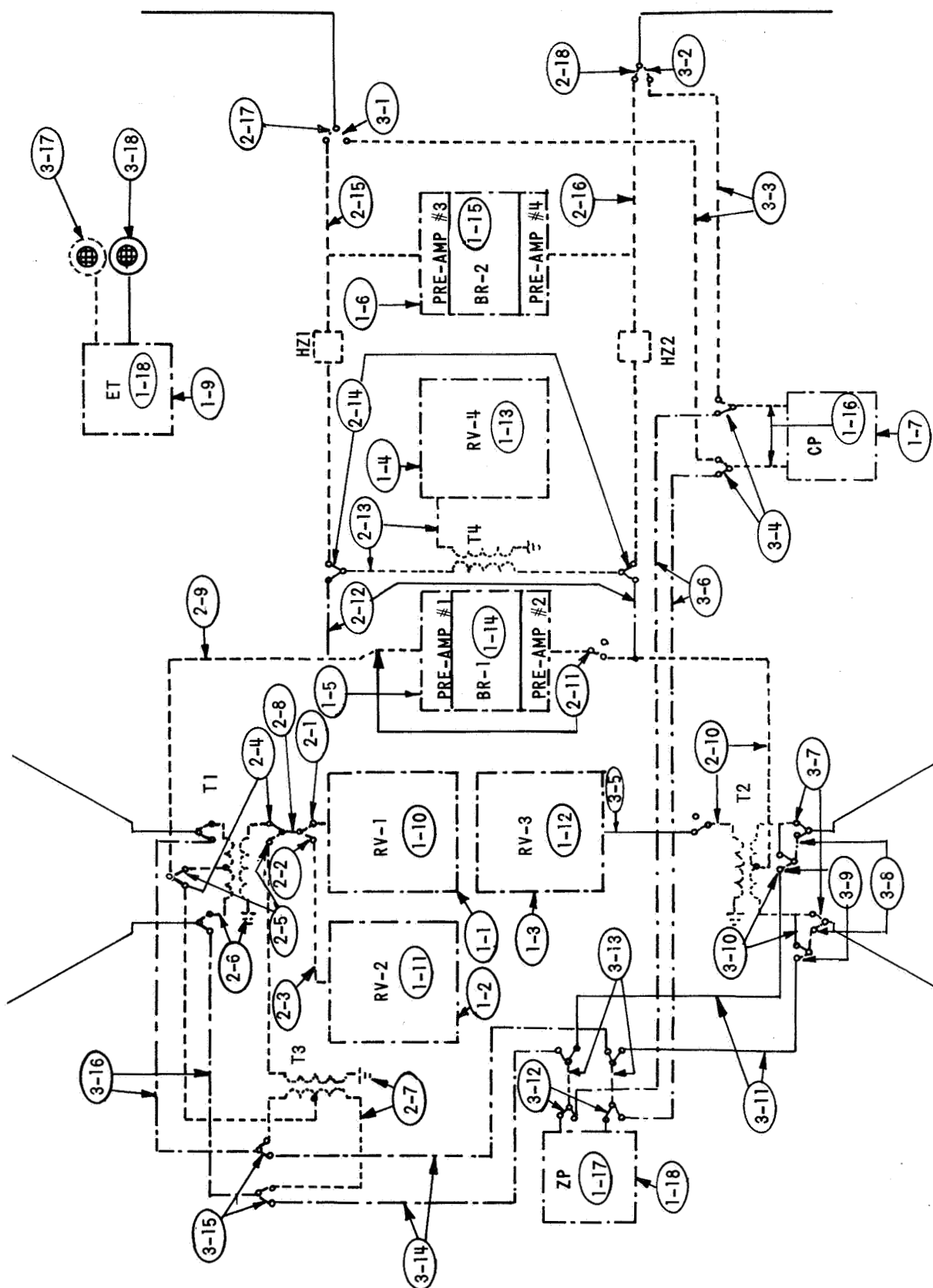


Figure III-10 ELECTRICAL TERMINAL CODE

IV. THIN FILM DESIGN TECHNIQUES FOR PEL MOSAIC DISPLAYS

A multi-diagram PEL display can be made by employing thin film deposition techniques. Such a display would employ an X-Y coordinate PEL cell structure, with insulated cross-overs for the voltage feed lines and access terminals to the two axes located along the edges of the substrate.

In order to produce a PEL X-Y mosaic display of high resolution, the individual cell elements must be constructed with a fine line high conductivity structure. Vacuum deposited coating, when processed by etching and subsequent electroplating, have produced fine line, high conductivity grids and circuits in previous experimental studies on micro-interconnections⁵. Figure IV-1 illustrates a PEL cell element in an X-Y cross-over mosaic structure.

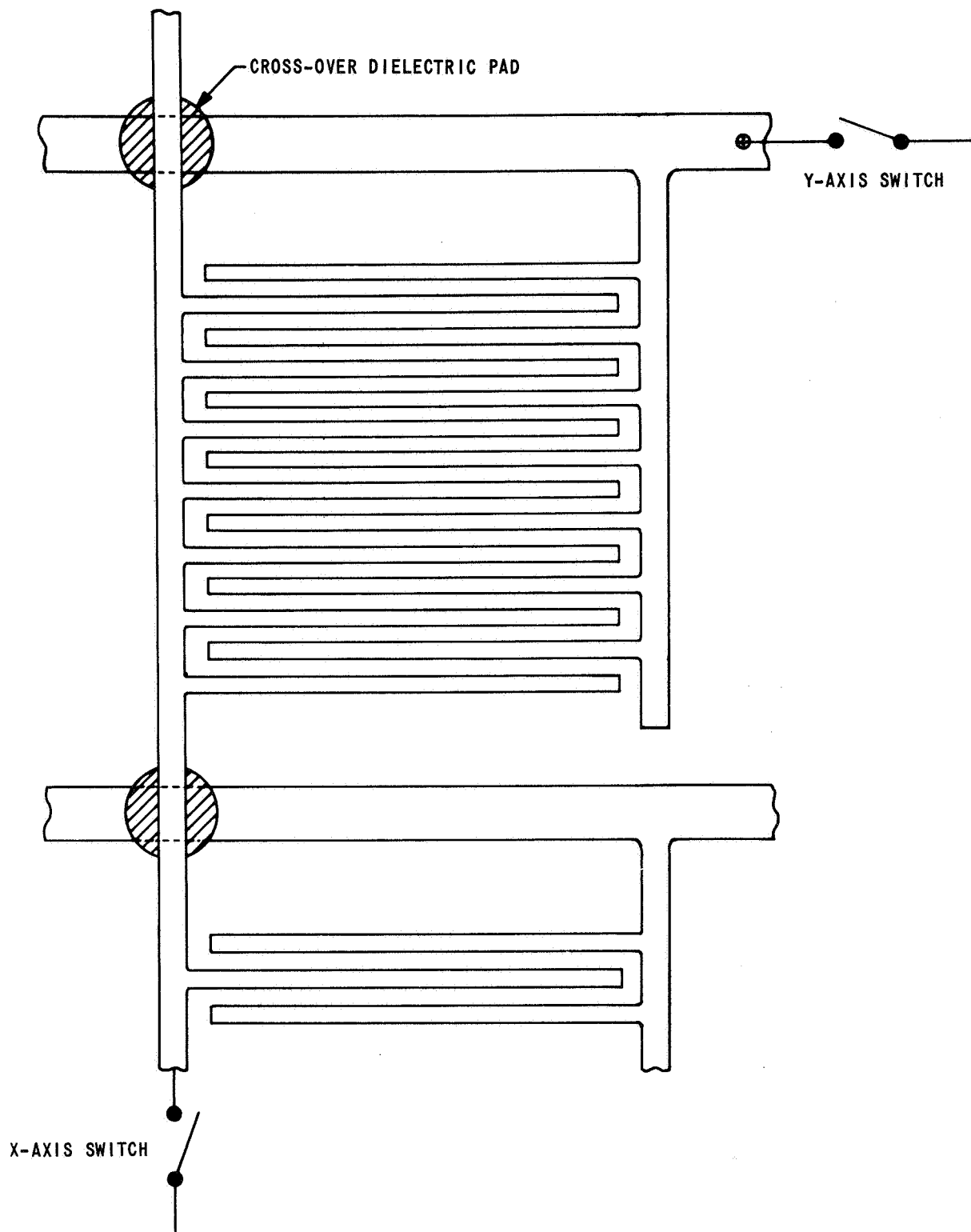


Figure IV-1 DETAIL OF INSULATED CROSS-OVER IN x-y MOSAIC

V. CONCLUSIONS AND RECOMMENDATIONS

The results of this program show that the planar electroluminescent concept can be used in large-area configuration displays having more than one color. While the EL phosphor formulations developed thus far have not achieved the optimum maintenance of brightness with time, further investigations in planar phosphor formulations are promising, in that there are a variety of systems not tested as yet.

It is recommended that a follow-on program be initiated for the development of techniques for the fabrication of large area, planar multi-diagram EL displays capable of storing the image for any length of time. In addition, it is also recommended that experimental and theoretical research be continued on the studies of the characteristics of EL generated as a function of the operating conditions of the displays.

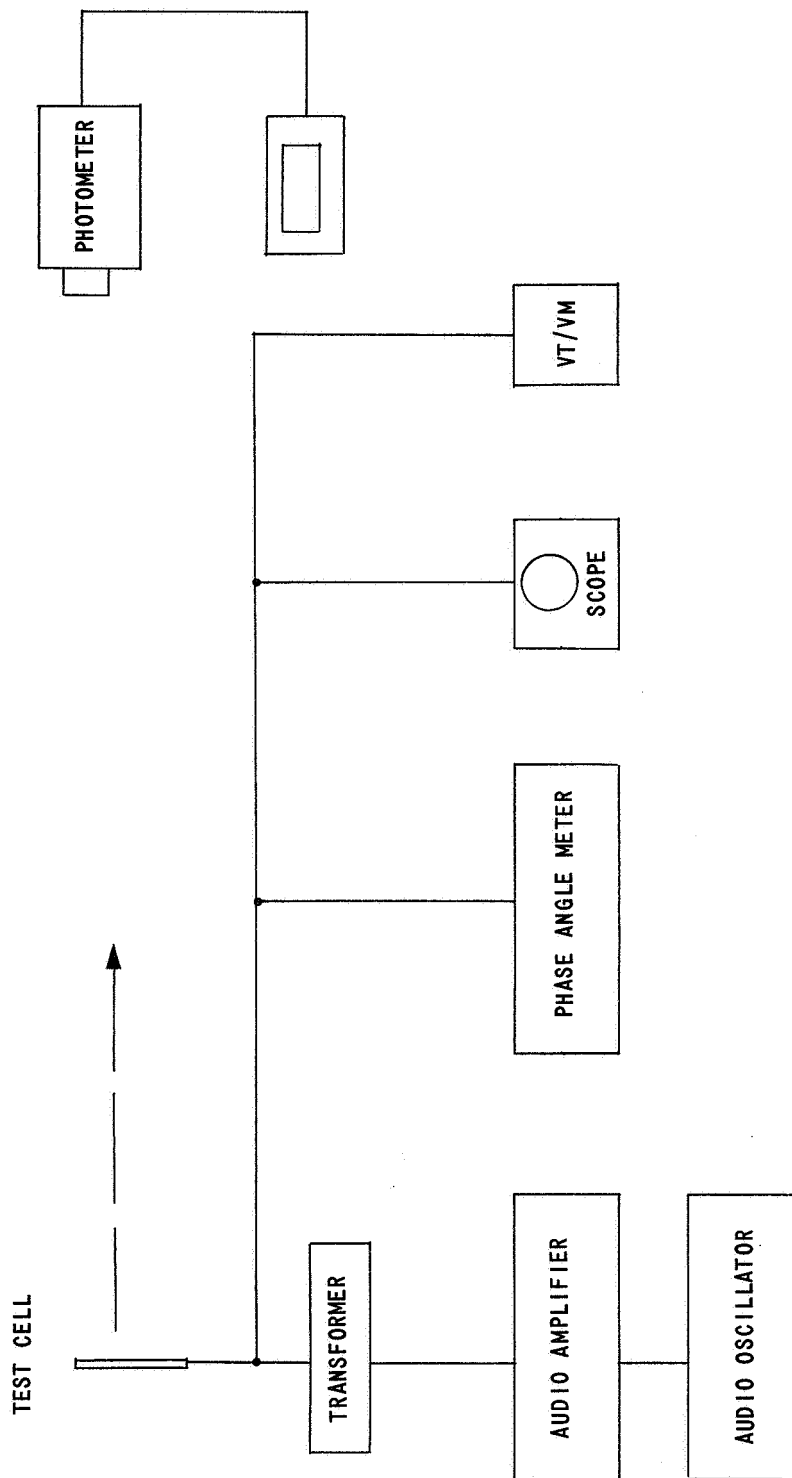
APPENDIX I-1

TEST CELL PERFORMANCE MEASUREMENTS

The performance of each test cell was evaluated by monitoring the following parameters:

1. Cell brightness (foot Lamberts)
2. Applied voltage (RMS)
3. Applied frequency (Hertz)
4. Electrical phase angle (Degrees)
5. Waveform characteristics - oscilloscope monitor

The tests were performed in the Laboratory white-room with controlled temperature, humidity, and dust conditions. Each cell was given the standard test sequence of initial brightness followed by a life test.



BLOCK DIAGRAM OF EL CELL TEST SETUP

APPENDIX II-1

ETCHING AND SILK SCREENING TECHNIQUES

Etching Techniques

The investigation of etching copper laminated to fiberglass filled epoxy boards has resulted in etchings of lines 4.0 mils wide with 4.0 mils spacing. The attempts to deposit phosphors by silk screening were first made with crude equipment and the results were far from consistent. A silk screen machine was purchased and first run testing appears satisfactory.

1. Etching

The copper laminate boards used were manufactured by General Electric Company and are rated as 1 oz. boards. The copper thickness is 1.3 mils as supplied. The boards were first cut to working size, then processed in the following fashion:

- a) One minute in water detergent solution under ultrasonic agitation.
- b) Three minute etch in 5% solution of hydrochloric acid.
- c) One minute rinse in running tap water.
- d) Vapor degrease for approximately one minute, repeat three times with air blast cooling between each vapor degrease cycle.
- e) Use a 70% by volume solution of 42° Baume ferric chloride etching solution and 30% tap water.
- f) The board is then etched for 16 minutes total time with the following procedure:
 - 1) Two minute etch (no agitation)
 - 2) One minute rinse in tap water

- g) After tap water rinse and while the board is still wet, repeat Steps b) and c).
- h) Dry board in a dry nitrogen blast with the regulator set for 40 psi.
- i) Examine the board for pin holes, foreign inclusions, and other defects which may require rejection of the substrate.
- j) Air dry the substrate with an infrared lamp for fifteen minutes.
- k) Clean the substrate of all dust with the electrostatic brush and spray coat with Kodak Photo Resist (KPR) in red safe light illumination and dust-free conditions.
- l) Air dry for thirty minutes in red safe light or no illumination.
- m) Place the substrate and transparency, emulsion side next to substrate, in the vacuum frame. Expose to the mercury arc lamp for ten minutes.
- n) Develop with Kodak Photo Resist Developer for two minutes and rinse immediately under running tap water at approximately 120°F.
- o) Dry in nitrogen blast at 30 psi and bake the substrate under the infrared lamp for at least thirty minutes.
- p) Inspect the substrate and KPR under the microscope to determine if the board is ready for final etching.
- q) Etch in the same solution as used in Step e) with frequent removal and tap water rinses to determine when the etching is complete.
- r) Repeat Steps b), c) and o).
- s) If the d.c resistance between electrodes is below 100 megohms, repeat Step d).
- t) The work is now ready for a protective coating of KPR. Follow Steps k) and l), however, the safe light precautions are not required. After drying, expose the substrate to the mercury arc for ten minutes and recheck the resistance.

If all tests and a visual inspection prove satisfactory, the substrate is ready for silk screening of the phosphor.

2. Silk Screening of Phosphors

The silk screening of phosphors has proven more an art than a science with the experience gained to date. The phosphor grain size of different phosphors will determine the minimum screen mesh which may be used with that grain size and the viscosity of the phosphor/binder ratio used. An emulsifying agent (silica gel) has been used when the phosphor settles from the binder rapidly. As each phosphor/binder ratio behaves differently, the amount of thinner must be governed by the worker's experience with the phosphor/binder/thinner used.

REFERENCES

- 1) "Electroluminescence and Related Effects", Henry F. Ivey, Academic Press, 1963.
- 2) CAL Disclosure No. 796; U.S. Patent Application Serial No. 246,981, filed December 1962. NOTE: All claims were allowed; patent will be issued early in 1967.
- 3) "Electroluminescence", H. K. Henisch, Pergamon Press, 1962.
- 4) Proceedings of the IRE, December 1955, Solid-State Electronics Issue, Vol. 43, No. 12.
- 5) "Microcable - A Novel Interconnection Technique for Micro-system Circuits", Proc. 4th Annual Microelectronics Symposium, St. Louis Section IEEE, May 24-26, 1965, St. Louis, Missouri.